ABSTRACT OF THE DISCLOSURE

A synchronous DRAM has a test mode wherein a specified external signal is input to a command decoder of the DRAM. The command decoder generates a plurality of internal commands including activating signal for selecting a word line, write signal, precharge signal, another activating signal and read signal at consecutive timings which do not depend on an external clock signal. A low-speed memory tester can be used for testing the high-speed synchronous DRAM.